Application Note, V1.3, September 2008

AP16103

XC2000/XE166 Family

Pin Configuration, Power Supply and Reset

Microcontrollers

Never stop thinking

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Page	Subjects (major changes since last revision)
all	Extended to XC2000/XE166 family

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1 Introduction

Infineon Technologies offers with the XC2000 and XE166 family a new generation of 16-bit microcontrollers based on the high-performance C166S V2 core. Both families provide new features to reduce system costs. This application note focuses on basic hardware related features such as EVR (Embedded Voltage Regulator), PORST (Power On ReSeT) and the configuration of special function pins. This application note (AP16103) covers the functionality of the following devices:

- xxx-XC228x-xxFxxLxx
- xxx-XC226x-xxFxxLxx
- xxx-XC238x-xxFxxLxx
- xxx-XC236x-xxFxxLxx
- xxx-XC2786X-xxFxxLxx
- xxx-XC2766X-xxFxxLxx
- XE167x-xxFxx
- XE164x-xxFxx

2 How to do a basic configuration

For correct operation the connection of several pins must be considered:

- **Test (/TRST, /TESTM)**
- **Power (TREF, VDDIM, VDDI1,VDDPA, VDDPB,VSS)**
- **Reset (/PORST, ESR0, ESR1,ESR2)**
- **Start-up (Port 10)**

2.1 Test

The pin **/TESTM** enables factory test modes. For normal operation it must be connected directly to VDDPB (Digital Pad Supply Voltage For Domain B). The pin **/TRST** is used to activate the debug system. For normal operation, it should have a pull-down resistor to Vss (Digital Ground). A high level at this pin plus a rising edge of /PORST activates the debug system.

2.2 Power

The device operates in the voltage range of 3.0V to 5.5V. The on-chip embedded voltage supply, consists of two separated voltage regulators VDDIM and VDDI1, these generate the core voltage of 1.5V. Various power down modes can reduce the power consumption of the core logic.

There are two groups of I/O pins. Optionally it is possible to operate both groups with the same voltage or with different voltages. For example the A/D conversion and some pins need 5 Volt and an external data memory needs 3.3 Volt. In this case the pin **VDDPA** (Digital Pad Supply Voltage for Domain A) is connected to 5 Volt and the pins **VDDPB** (Digital Pad Supply Voltage for Domain B) are connected to 3.3 Volt.

The pin **TREF** (only AA-Step) works as a control pin for the core voltage generation. To activate the embedded on chip voltage supply pin TREF must be connected to VDDPB. This connection is no longer required from step AB on. For the current step, pin TRef is logically not connected. Future derivatives will feature an additional general purpose IO pin at this position.

The embedded voltage regulator is divided in domain M (pin **VDDIM**) and domain 1 (**VDDI1**). In low power mode domain 1 can be switched off for power reduction. The pin VDDIM should be connected with a ceramic capacitor of at least 1µF. The maximum value of 4.7µF should not be overstepped. All pins VDDI1 should be connected to each other; each pin needs a 470nF ceramic capacitor. The maximum value of 2.2µF for each voltage domain 1 should not be overstepped.

2.3 Reset

The pins **/ESR0**, **/ESR1** and **/ESR2** can serve as an external reset input as well as a reset output (open drain) for (internal) application resets. By default, reset functionality of /ESR1 and /ESR2 are disabled and an internal weak pull up resistor is active. For these pins there is no special recommendation about the configuration. By default the /ESR0 is configured as a bidirectional pin with pull up device. The pin /ESR0 serves as an external reset input as well as a reset output (open drain) for (internal) application reset. After reset an internal weak pull up resistor is active for /ESR0. To reduce noise sensitivity of /ESR0 it is recommended to use either a block capacitor (100nF) to ground or use an external pull up resistor to tie the pin to VDDPB. In register RSTCON1 the reset function of /ESR0 can be disabled.

The supply voltage VDDPB is monitored to validate the overall power supply. The supply watchdog detects ramp up or ramp down of the external supply voltage and generates a power on reset. Thanks to this module only a simple low cost (3 pin device) voltage regulator is needed. Up to 16

selectable threshold levels from 2.9 Volt to 5.5 Volt allow to monitor the external power supply and can generate, if mandatory, an interrupt or reset.

For debugging it is recommended to use a pull up resistor to tie **/PORST** to VDDPB. If an additional power on reset is requested the pin /PORST must be driven low. /PORST is equipped with a noise suppression filter that suppresses glitches below 10 ns pulse width. /PORST pulses with a width above 100 ns are safely recognized.

2.4 Startup Mode

In order to assure a proper startup from the internal flash two pins of the port P10 needs to be configured. Pin P10.0 and P10.1 have to be connected via resistors to VDDPB.

To select different startup modes like UART/SPI/CAN Bootstrap Loader some dedicated pins on Port10 have to be configured.

The different modes can be triggered after a power-on reset or an (internal) application reset:

- **Start from internal Flash: Pins 10.1-10.0 are sampled as 11B**
- **Activate ASC BSL: Pins 10.2-10.0 are sampled as 110B**
- **Activate CAN BSL: Pins 10.2-10.0 are sampled as 101B**
- **Activate SPI BSL: Pins 10.3-10.0 are sampled as 1001B**

2.5 Configuration Example

Figure 1 illustrates how such a configuration can look like. The values for the oscillator circuit are dependent on the crystal type used. The resistors “optional” are needed if the debug interface is used.

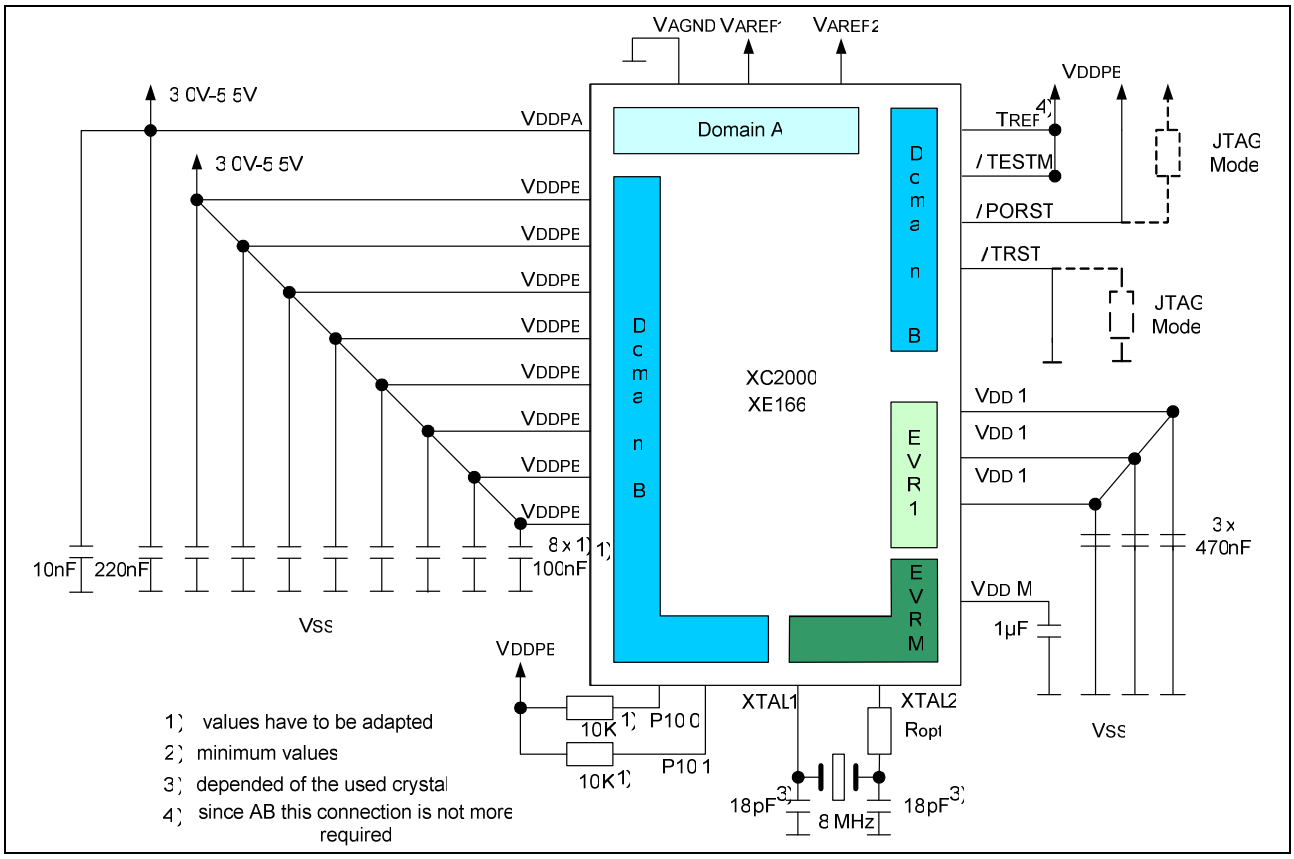

Figure 1 Configuration example “Internal Start from Flash”

Capacitor	Supply	Pins (QFP-144)	Pins (QFP-100)
100nF	VDDPB	2	2
100nF	VDDPB	36	25
100nF	VDDPB	38	27
100nF	VDDPB	72	50
100nF	VDDPB	74	52
100nF	VDDPB	108	75
100nF	VDDPB	110	77
100nF	VDDPB	144	100
>= 1 µF*	VDDIM	15	10
220nF	VDDPA	20	14
>= 470nF**	VDDI1	54	38
>= 470nF**	VDDI1	91	64
>= 470nF**	VDDI1	127	88

Table 1 Decoupling Capacitor List

* For AB-Step = 1µF (For all other steps the capacitance value should be in the range of 1µF up to 4.7µF)

**For AB-Step = 470nF (For all other steps the capacitance value should be in the range of 0.47µF up to 2.2µF)

For better power dissipation, a package with exposed pad is offered. To reach the minimum thermal resistance Junction-Ambient (<= 22K/W) a 4-layer board with thermal vias should be used. The exposed pad needs to be soldered and tied to ground.

3 Power supply

Monitoring the external power supply allows the usage of a low-cost regulator without additional status signals. The chapter discusses the following items:

- **Single power supply**
- **Dual power supply**

3.1 Single power supply

Typically most systems need only one power supply. With the embedded voltage regulator and the supply watchdog, a 3 pin low cost voltage regulator meets all requirements.

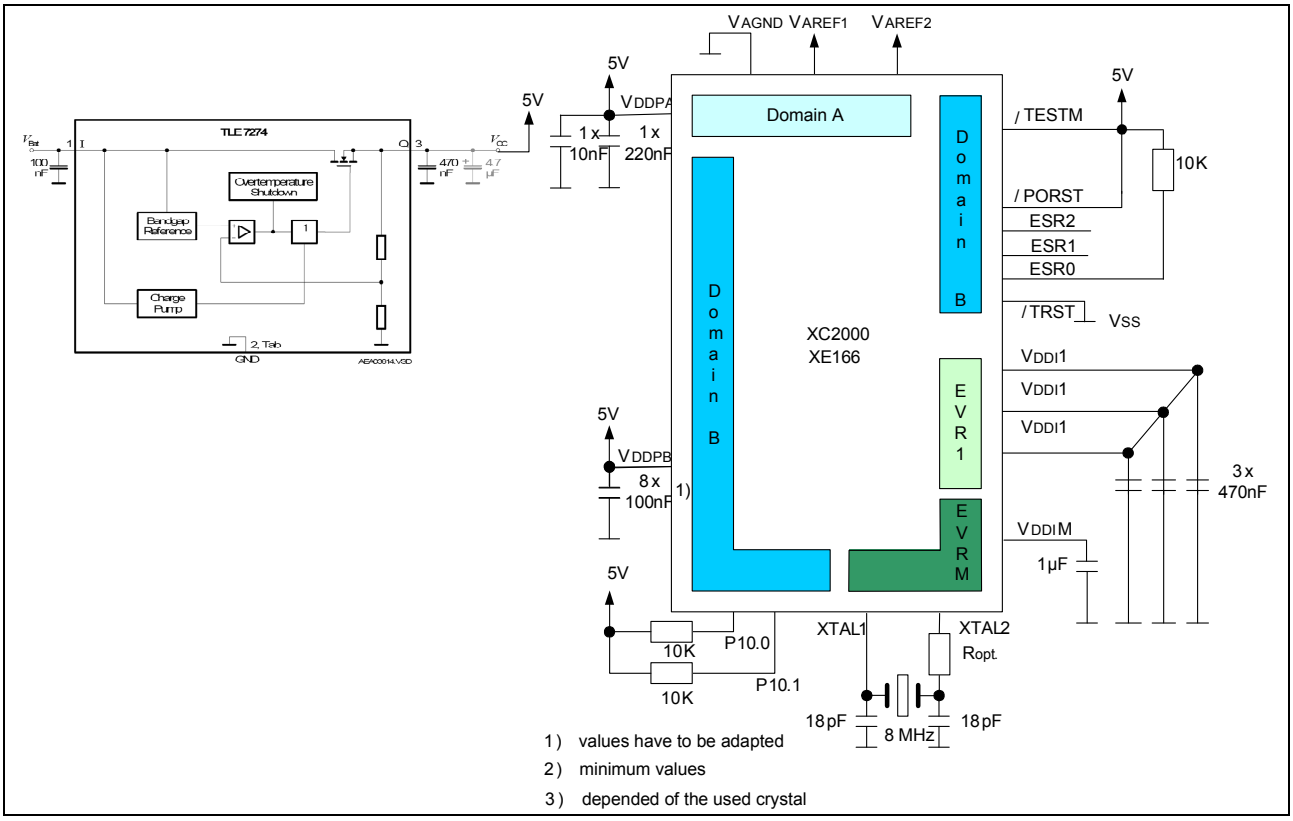

Figure 2 Single power supply using the TLE7274

The TLE 7274 is a monolithic integrated low-drop voltage regulator for load currents up to 300 mA. An input voltage up to 42 Volts is regulated to VQ, nom = 5.0 Volts with a precision of ±2%. The stand-by current consumption is typically 20µA. Therefore the device is dedicated for use in applications which are permanently connected to VBAT.

If the system can be switched off completely, the TLE 7276 can be chosen. This voltage regulator has an additional control pin (Inhibit) that disables the 5 Volt.

3.2 Dual power supply

Some applications require two external voltage domains. One reason can be that the board voltage supply is 3.3 Volts but some external components, like sensors provide 5 Volt signals. The XC2000/XE166 family supports such requirements with their flexible voltage domain concept.

The digital supply voltage for domain B and the embedded voltage regulator is supplied with 3.3 Volts, the domain A is supplied with 5 Volts. The domain B supplies all ports, except Port5, Port6 and Port15, with 3.3 Volts. To assure that both voltage sources are nearly synchronized the inhibit functionality is used. The total power dissipation is explicitly reduced.

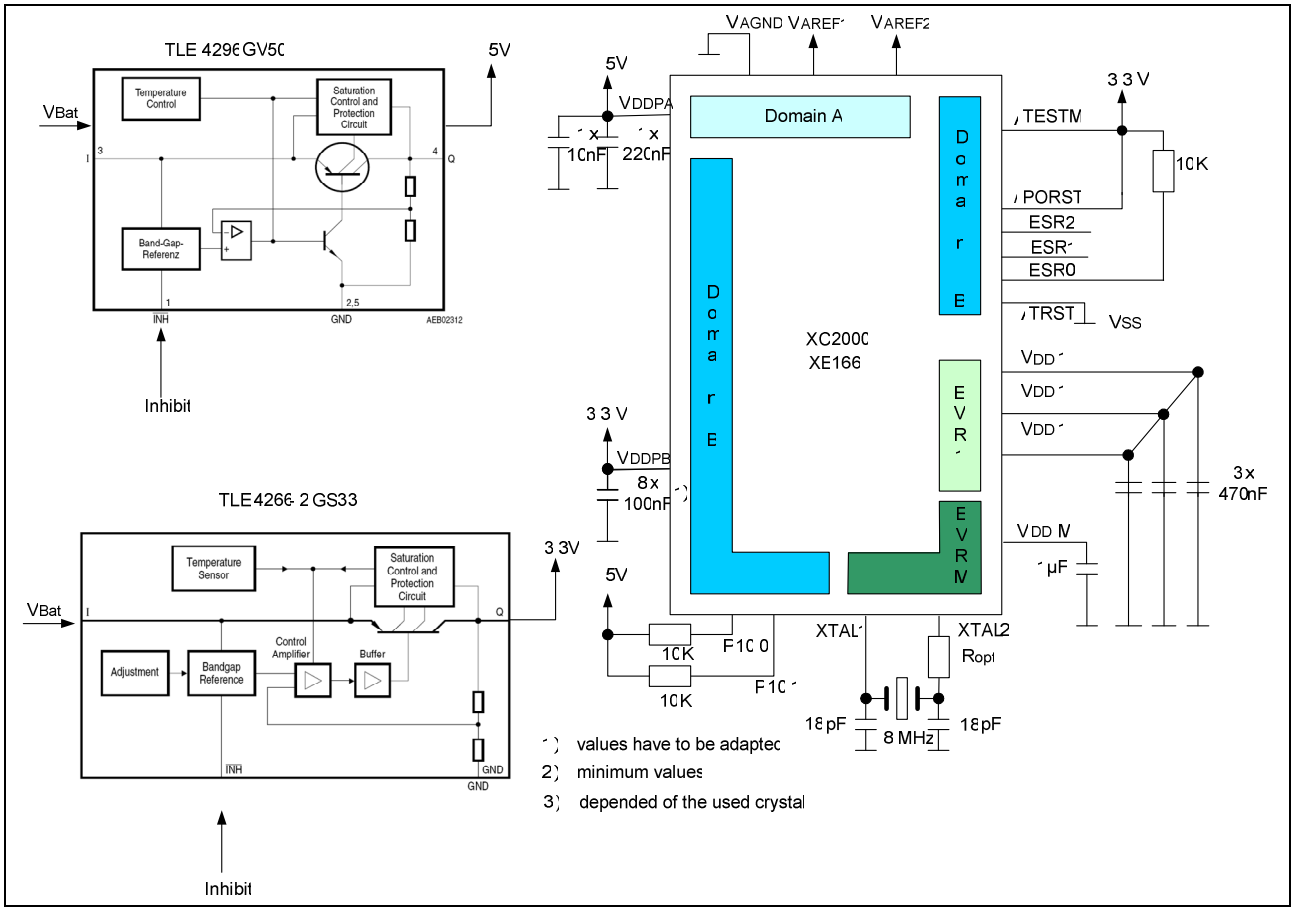

Figure 3 Dual power supply using TLE4296 GV 50 and TLE4266-2-GS33

The TLE 4296-2 G is a monolithic integrated low-drop voltage regulator in the very small SMD package P-SCT595-5. The output is able to drive a load of more than 30 mA while it regulates the output voltage within a 4% accuracy.

The TLE 4266-2 is a monolithic integrated low-drop fixed voltage regulator which can supply loads up to 150 mA.

4 Special Reset configurations

4.1 Using ESR pins to trigger a PORST reset

In some Application Software or Hardware states (TRAPS or exceptional hardware events) it is required to do a Power on Reset. Since the XC2000/XE166 can not trigger a PORST via software or internal Hardware an external connection need to be used.

The ESR pins serve as multi-functional pins with a huge amount of different options, such as reset input/output. After power on, ESR0 is configured as reset input for an internal application reset in open drain mode. ESR0 drives an active low signal after power on for the time the internal reset counter is running (see figure 5). For this reason ESR0 can not be directly connected to the /PORST pin.

ESR1 and ESR2 are configured after start up as normal input pins, Pull-up device activated. One of the two pins could be connected directly to the /PORST pin (Figure 4). To trigger a PORST the register ESRCFG1 or ESRCFG2 of the respective ESR pin needs to be written with the corresponding value for reset output drives, a 0 for an Internal Application or Application Reset in open drain mode. The Reset counter RSTCNTA in register RSTCNTCON should be set to the maximum value. The ESR Pin could be used as well as I/O pin so that the Software could trigger a PORST by setting the respective ESR pin to 0 to achieve a proper external reset pulse outside. If the Watchdog Timer should trigger a PORST, the ESRCFGx register needs to be setup for the same type of reset like the WDT.

In some Applications with a higher Safety level, an external Supply Watchdog is used. Figure 4 shows that the /RESETIN of the Supply Watchdog can be used to trigger a PORST.

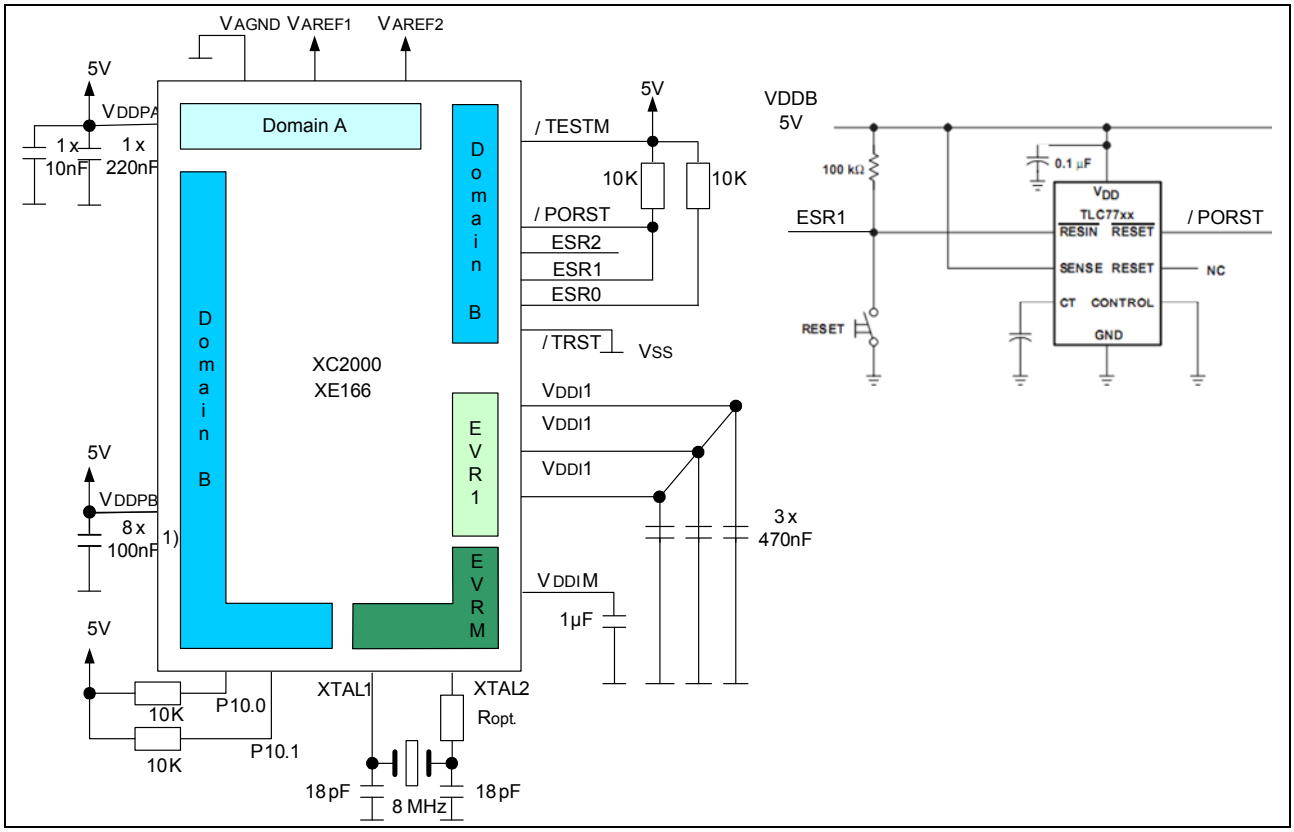

Figure 4 Trigger a PORST with the ESR1 pin

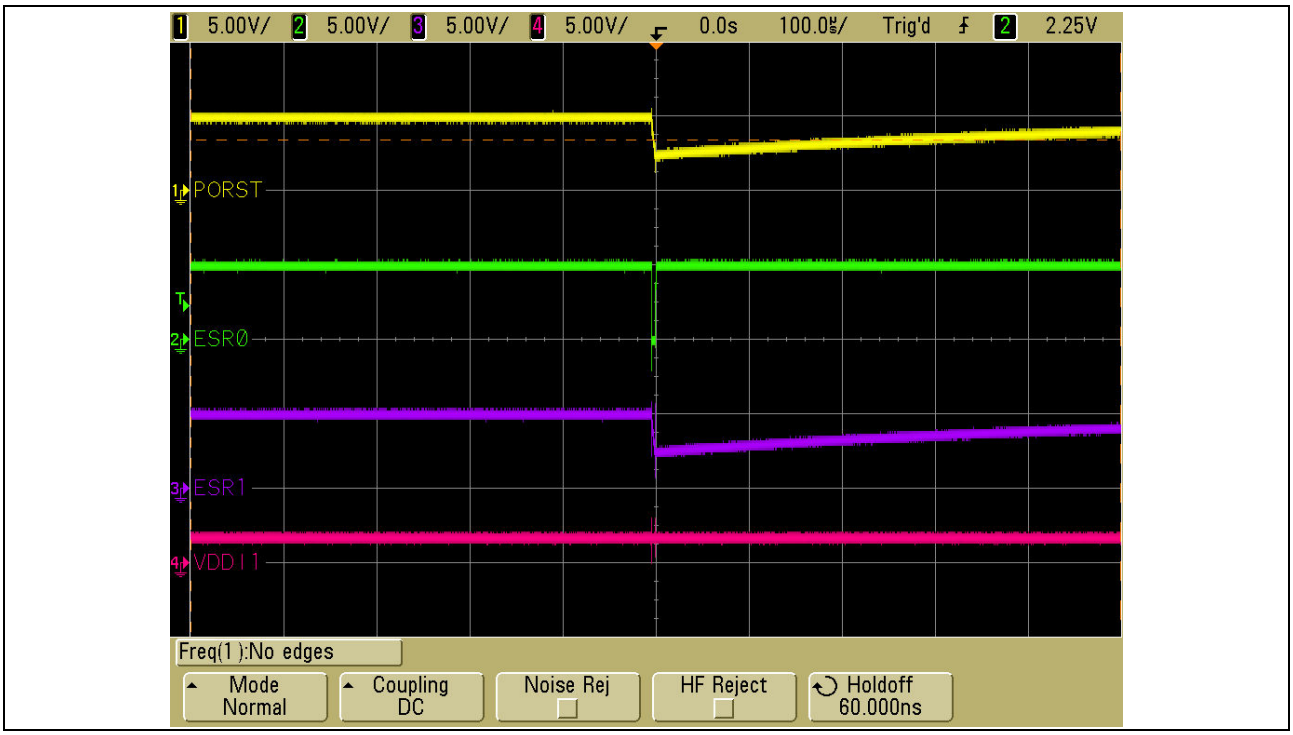

Figure 5 Trigger a PORST with the ESR1 pin

4.2 Using ESR pins for reset out delay (RSTOUT)

Some Applications require a reset out signal together with a reset out delay after power up as long the initialization is done. The XC166 family had a special pin for this function, the RSTOUT pin (Figure 6). The new XE166 offers a wide range of reset functions wich can be used in the same way as known from the 16Bit family.

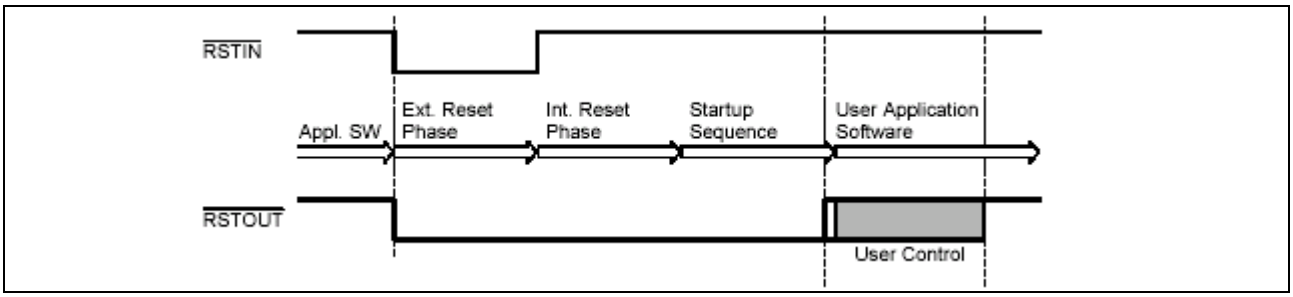

Figure 6 RESET out of XC166

The ESR pins serve as multi-functional pins with a huge amount of different options, such as reset input/output. ESR0 is configured as reset input (active low) after power up. For this reason ESR0 can not be used as the RSTOUT signal.

ESR1 and ESR2 are configured after start up as normal input pins, Pull-up device activated. One of these Pins can be used together with an external Pull down to hold the signal at a low level. Later in the application software the pin can be switched to Push-pull output driving a high level. In Figure 7, the SCU_ESRCFG1 was written with a 0x000A; at the end of system init.

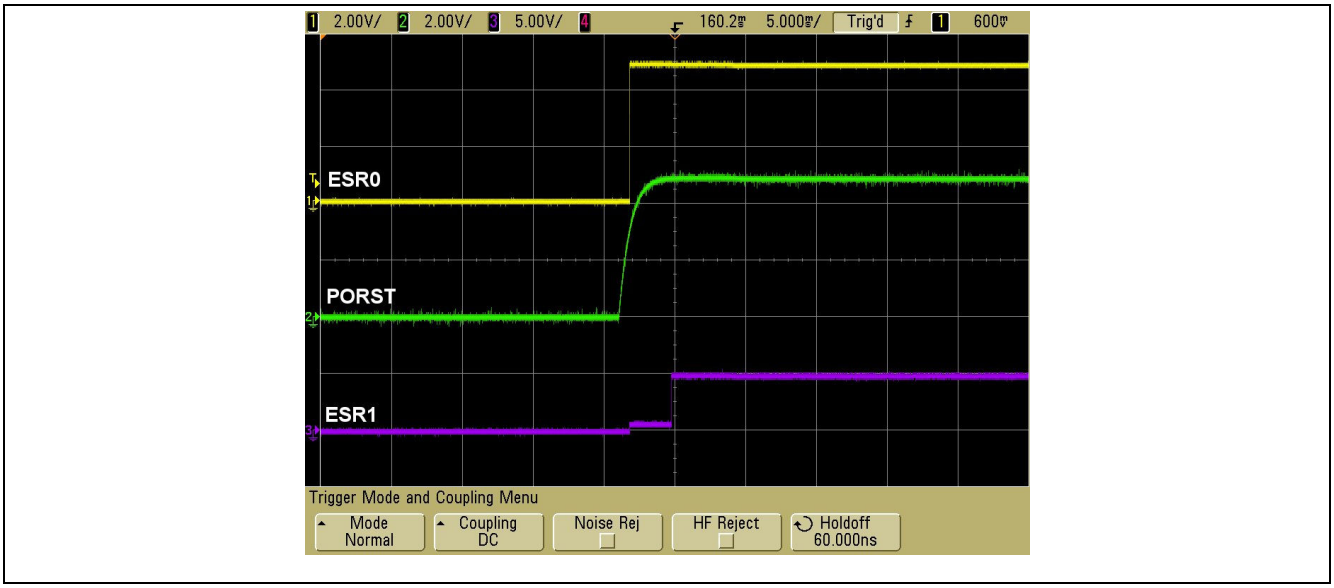

Figure 7 ESR1 as reset out signal with reset out delay after power up

5 Conclusion

The XC2000/XE166 family supports several powerful mechanisms such as embedded voltage regulator, power on reset, two independent voltage domains and supply watchdog to address different application scenarios. Following the family concept Infineon Technologies is able to offer a wide range of different devices to meet the diverse requirements of the market.

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